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RESEARCH ARTICLE OPEN ACCESS

Cascaded H-Bridge Multilevel Inverter in a Single-Phase eleven level

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Abstract—
This paper basically concentrates on the design and implementation of new topologies for a single phase eleven level cascaded H-bridge multilevel inverter by using different kinds of switching schemes. The main purpose of this paper is to increase the number of voltage level at the output without addition of any complexity to power circuit. The main advantages of this proposed topology is to reduce the THD and less electromagnetic interface EMI generation and high voltage with very nearer to sinusoidal waveform. In this paper, various kinds of carrier pulse width modulation techniques are proposed as which minimize the total harmonic distortion and improve the out voltage from the proposed technology and POD modulation techniques reduce the THD at lower. A number of H-bridge arranged in cascaded manner to increase the voltage level with the different switching schemes analyzed in this paper. It is observed that this new topology can be recommended to single phase eleven level cascaded H-bridge inverter for better and enhanced performance over the conventional methods.The simulation model is created by MATLAB2009 software version. Index Term- Cascaded H-bridge Multilevel inverter, different phase pulse width modulation, lower total harmonic distortion, EMI
Keywords—Multi-level inverter, RV topology and carrier phase-shifted PWM.

I. INTRODUCTION

A multilevel inverter is a power electronic device that is used for high-power high-voltage applications such as Uninterruptible power supplies, flexible ac transmissionsystems, and high voltage dc transmission systems. Whereas conventional two level inverter have some limitations in highpower
high-voltage applications due to switching losses and power ratings [1-2]. Multi-level power conversion is provided more than two voltage levels to achieve smoother and less distorted dc to ac power conversion and it can generate a multiple-step voltage waveform with less distortion, less
switching frequency and higher efficiency. The stepped waveform is synthesized by multiple voltage levels generated by the proper connection of the load. This connection is performed by the proper switching of the power semiconductors. To obtain a quality output voltage waveform they require high switching frequency along with different pulse-width modulation strategies [3]. Multi-level inverter offers several advantages over two-level inverter hence improves the output voltage waveform, reduced (dv/dt) voltage stress on the load and also reduces electromagnetic interference problems, but it has some disadvantages. One of the most obvious disadvantages is the requirement of higher number of power semiconductor switches. Every switch requires a gate driver circuit, therefore increasing the complexity and size of the overall circuit [4]. Lower voltage rated switches can be used in multi-level inverter instead of higher number of semiconductor switches which can be minimized cost of the semiconductor switches as compared to two level inverters. The multilevel cascaded H-bridge (CHB) inverter shown in Figure 2.1 is one of the popular inverter topologies for highpower
applications due to its high voltage operating capability, low dv/dt with reduce total harmonic distortion (THD) and modular structure for reduced manufacturing cost [5]. The conventional modulation schemes for the multilevel CHB inverter include carrier based sinusoidal modulations with phase opposition disposition techniques [6, 7]. The levelshifted modulation schemes have a good THD profile, but suffer from unbalanced power distribution [8-10], whereas the phase shifted schemes are simpler but produce higher total harmonic distortion (THD) [8]

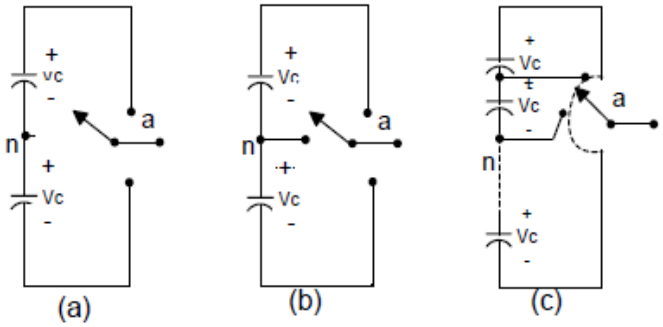
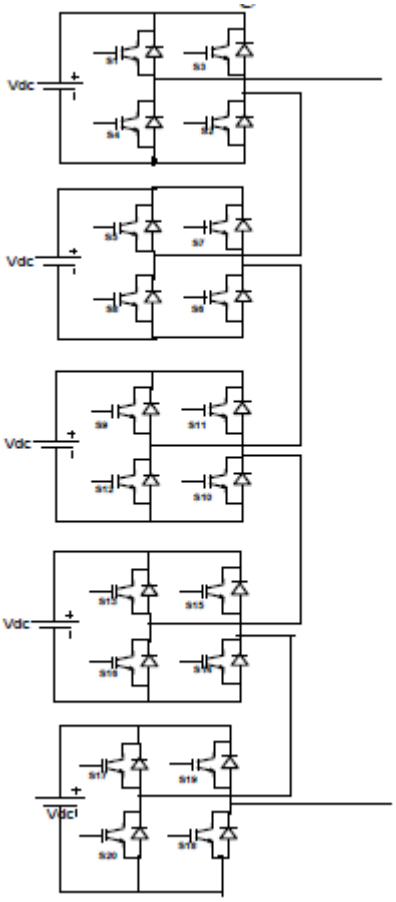


Figure 1: one phase leg of inverter (a) two level (b) three level (c) n-levels An equivalent representation of one phase leg of inverters with different levels shown in figure 1, and power semiconductors is represented by an ideal switch with several positions [3].

There are different conventional multi-level inverters topologies are neutral point- clamped, flying apacitors (capacitor clamped), and cascaded H-bridge (CHB). In 1981 Nabae Phase opposite disposition PWM scheme offers great advantages such as improved output voltage waveforms, lower
EMI, and lower THD in comparison of other PWM switching schemes.

II. PROPOSED TOPOLOGY

This topology requires twenty semiconductor switches and five isolated dc sources shown in fig 2.2 According to the table, there are eleven switching combinations to control the inverter and it shows the great redundancy of the topology.



OPERATION OF SINGLE-PHASE ELEVEN-LEVEL INVERTER ARRANGED IN CASCAD MANNER

Operation of the single-phase eleven-level inverter with CHB topology can be easily explained with the help of fig. 1.2 and table I.

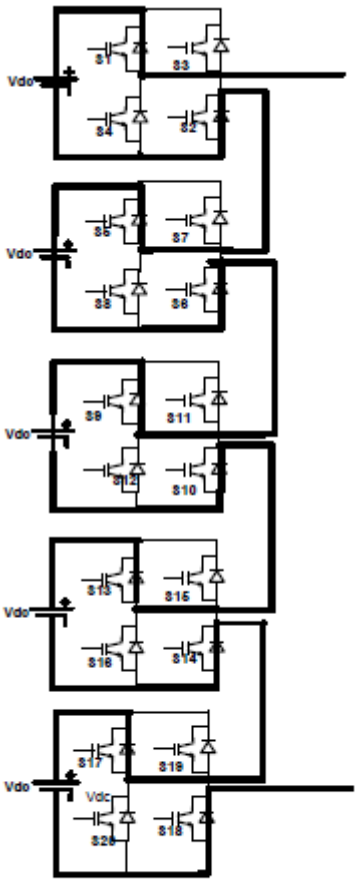
When switches S1,S2, S6,S8,S10,S12,S14,S16,S18 and S20 are turned "on" the output voltage will be "Vdc" (i.e., level 1). The output voltage will be "2Vdc" (i.e., level 2) when switches S1,S2,S5,S6,,S10,S12,S14,S16,S18 and S20ar e turned "on". When S1,S2,S5,S6,S9,S10,,S14,S16,S18 and S20 switches are turned "on" the output voltage will be "3Vdc" (i.e., level3). When switches S1,S2,S5,S6,S9,S10,S13,S14,S18 and S20 are turned on the output voltage will be "4Vdc" (i.e., level4).When switches S1,S2,S5,S6,S9,S10,S13,S14,S17,S18
and S20 are turned on the output voltage will be "**5**Vdc" (i.e.,level 5).
When switches S2,S4,S6,S8,S10,S12,S14,S16,S18 and S20 "on" the output voltage is zero (i.e., level 0).
S3,S4,S7,S8,S11,S12,S15,S16,S19 and S20 turn negative half cycle can be generated across load. The voltage blocking capacity of each switch is Vdc [2]. The operation of this topology can also be easily

understood by mode of operation of single-phase eleven-level inverter shown in figure 2. Each voltage source "Vdc" is required 100V. There are eleven sufficient switching modes in generating the multistep levels for a eleven-level inverter..

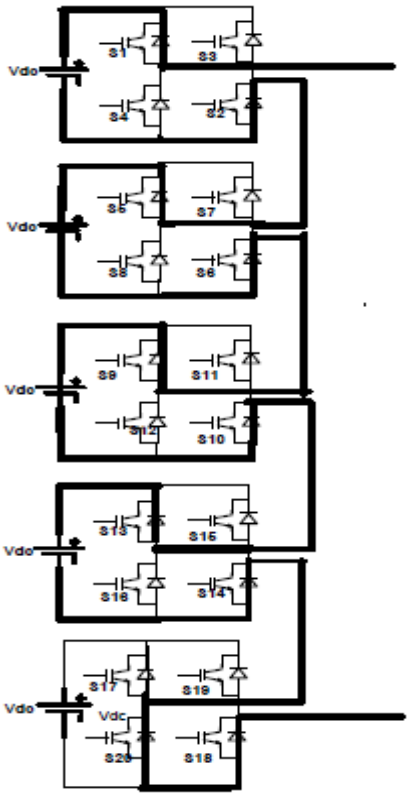
OPERATION MODE:

Operational modes for this topology is described in following manner, appropriate diagrams also shown below for this topology according to its operation

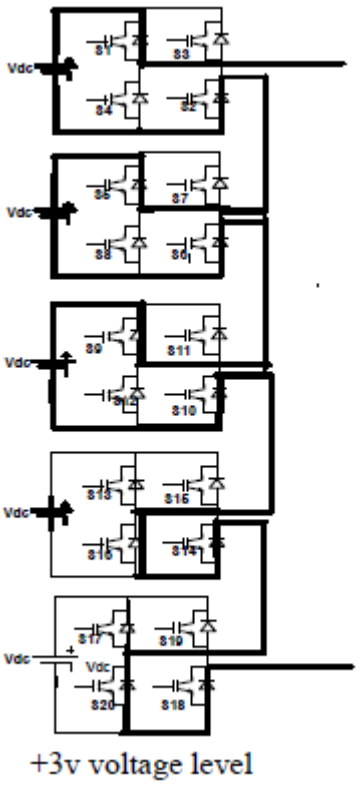
There are six modes of operation for representing the whole phenomenon implanting in this topology



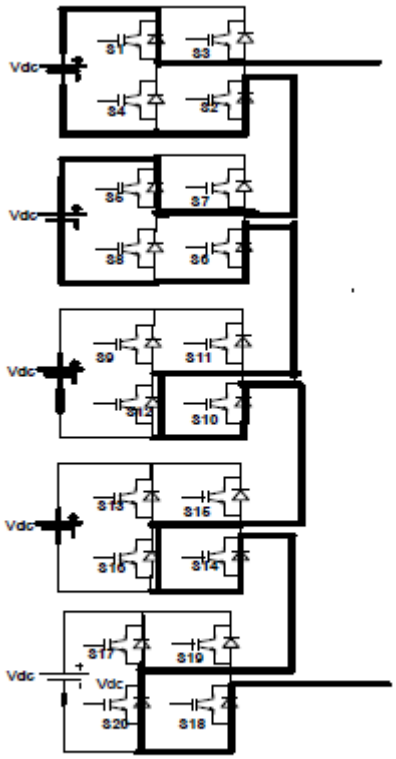
+5v voltage level



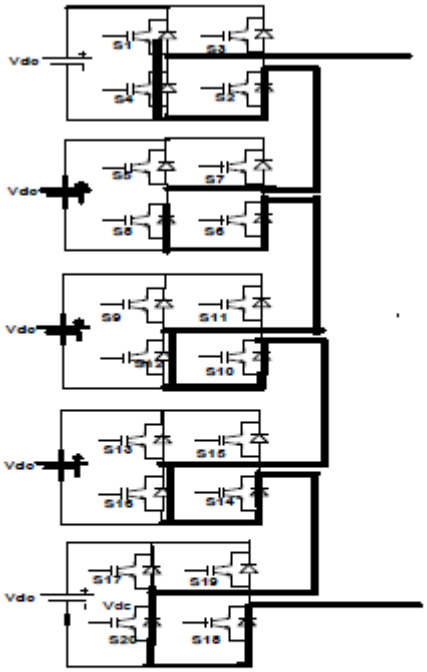
+4v voltage



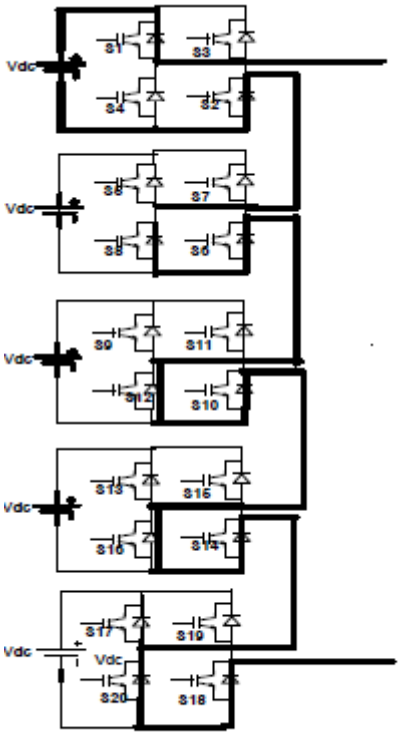
+3v voltage level



+2v voltage level



0 Level



Level 1v

LEVEL	SWITCH STATES																			OUTPUT VOLTAGE
	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16	S17	S18	S19	S20	
5	✓	✓			✓	✓			✓	✓			✓	✓			✓	✓			5Vdc
4	✓	✓			✓	✓			✓	✓			✓	✓				✓		✓	4Vdc
3	✓	✓			✓	✓			✓	✓				✓		✓		✓		✓	3Vdc
2	✓	✓			✓	✓				✓		✓		✓		✓		✓		✓	2Vdc
1	✓	✓				✓		✓		✓		✓		✓		✓		✓		✓	Vdc
0		✓		✓		✓		✓		✓		✓		✓		✓		✓		✓	0
-1			✓	✓		✓		✓		✓		✓		✓		✓		✓		✓	-Vdc
-2			✓	✓			✓	✓		✓		✓		✓		✓		✓		✓	-2Vdc
-3			✓	✓			✓	✓			✓	✓		✓		✓		✓		✓	-3Vdc
-4			✓	✓			✓	✓			✓	✓			✓	✓		✓		✓	-4Vdc
-5			✓	✓			✓	✓			✓	✓			✓	✓			✓	✓	-5Vdc

MODULATION STRATEGIES:-

There are different pulse width modulation with different phase relationships.

- Phase disposition pulse width modulation (PD PWM):- In phase disposition pulse width modulation strategy, where

all carrier waveforms are in same phase.

- **Phase opposition disposition pulse width modulation**

(**POD PWM**):- pulse width modulation (PS PWM**)**:-

Fig.3.1 shows the carrier Phase-opposition pulse width modulation strategy. In phase opposition disposition pulse width modulation strategy, where all carrier waveforms above zero reference are in phase and below

zero reference are 180_0 out of phase.

- Alternate phase opposition disposition pulse width modulation (APOD PWM):- In alternate phase opposition disposition PWM scheme where every carrier waveform is in out of phase with its neighbor carrier by 180_0

.

- Phase-shifted A carrier phase shifted PWM for multilevel inverter is used to generate the stepped multi-level output voltage waveform with lower % THD. In proposed, before implementing the Multicarrier PWM Techniques, the gating signals of multi-level inverter switches are generated by comparing sinusoidal reference wave with triangular carrier waves (N-1=3) with 120_0 phase displacement and a constant value at specific intervals of time

0 0.01 0.02 0.03 0.04 0.05-400-2000200400
Selected signal: 2.5

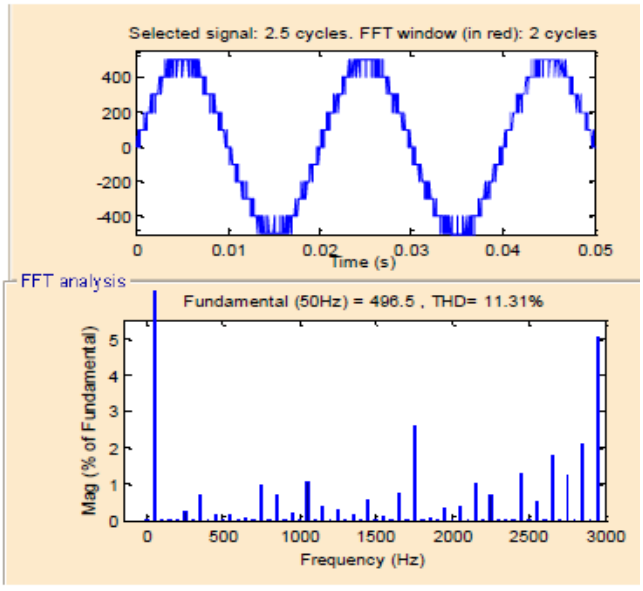
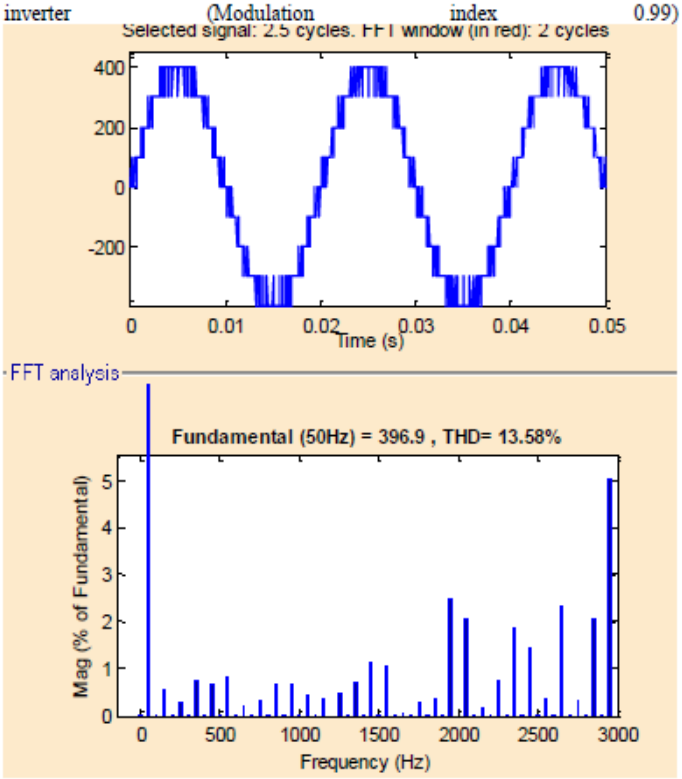


Figure 4.2: PWM output voltage and harmonic spectrum in CHB (Modulat index 0.99 (11level MLI)

Figure 4.3: PWM output voltage and harmonic spectrum in CHB 9LEVEL inverter (Modulation index 0.99)



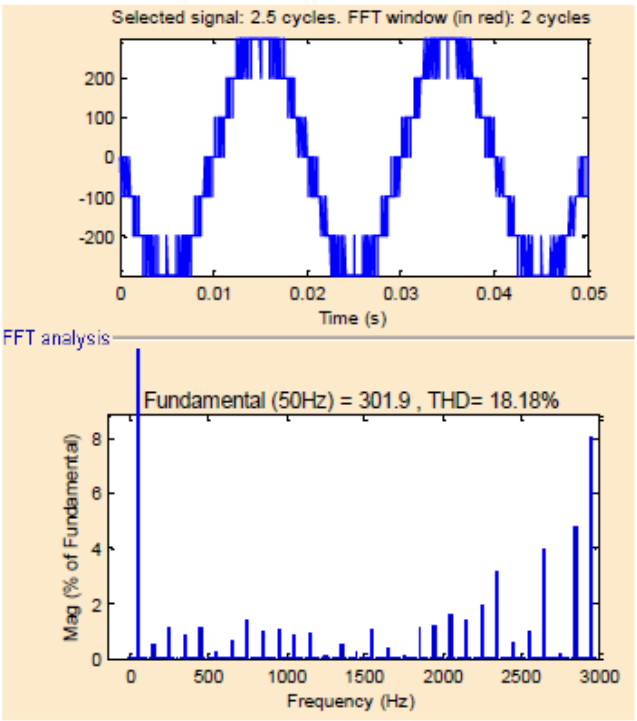


Figure 4.4 PWM output and harmonic spectrum in CHB 7level (MI 0.99)

III. CONCLUSION:-

Multi level cascaded H bridge inverters from 7-levels to 11- levels have been simulated using Matlab/Simulink. The following conclusions can be made from the analysis As number of level increases, the THD content approaches to small value as expected. Thus it eliminates the need for filter. Though, THD decreases with increase in number of levels, some lower or higher harmonic contents remain dominant in each level. These will be more dangerous in induction drives. Hence the future work may be focused on implementing closed loop control with suitable harmonic elimination.

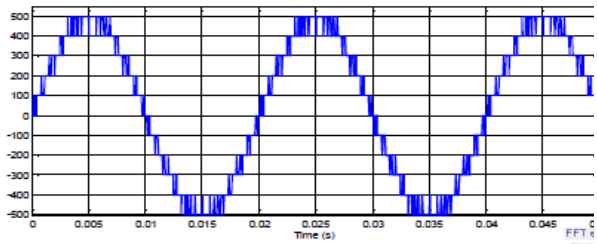
NUMBER OF COMPONENTS:- The number of required components for single-phase elevenlevel inverter is shown in Table II

TABLE-II

Inverter type	NPC	Flying capacitor	cascade	Proposed
Main switches	2(N-1)	2(N-1)	2(N-1)	(N-1)+4
Main diodes	2(N-1)	2(N-1)	2(N-1)	(N-1)+4
Clamping diodes	2(N-2)(N-1)	0	0	0
DC bus Capacitor/ Isolated supplies	(N-1)	(N-1)	3(N-1)/2	(N-1)/2
Flying capacitors	0	(N-1)(N-2)/2	0	0
Total numbers	(N-1)(2N+1)	(N-1)(N+8)/2	11/2(N-1)	(5N+11)/2

IV. SIMULATION RESULTS:-

In this topology, a carrier based phase shifted PWM scheme is used. The figure 2.2 shows the simulated model of singlephase eleven-level voltage inverter. Twenty IGBTs are used and each of the switches requires a separate gate driver circuit. The simulation parameters are as following R = 20 ohms, L = 10mH, and dc source voltage is 100V; Frequency of carrier signal is 3 kHz. Based on the PODPWM techniques, the harmonic spectrum was analysed using the FFT Window in MATLAB/Simulink. Table III shows THD comparison between different levels. When modulation Index vary between 0.5 and 1, it is called low modulation [09]



PERCENTAGE THD COMPARISON FOR DIFFERENT LEVELS

MODULATION INDEX	PWM %THD FOR 11-LEVEL	PWM %THD FOR 9-LEVEL	PWM %THD FOR 7-LEVEL
0.99	11.31	13.58	18.18
0.95	12.10	15.76	20.97
0.92	13.29	16.59	21.94
0.88	13.97	17.59	22.93
0.75	15.90	17.80	25.38

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